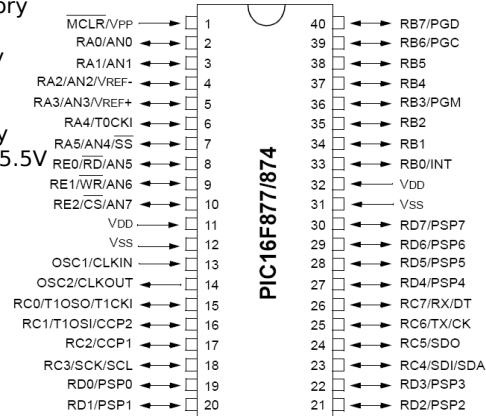


PIC 16F877

- High performance RISC CPU
- 35 single word instructions
- All single cycle instructions except for program branches
- Operating speed: DC - 20 MHz clock input
- 8K x 14 words of FLASH Program Memory
- 368 x 8 bytes of Data Memory (RAM)
- 256 x 8 bytes of EEPROM Data Memory
- Interrupt capability (up to 14 sources)
- Eight level deep hardware stack
- In-Circuit Serial Programming capability
- Wide operating voltage range: 2.0V to 5.5V
- High Sink/Source Current: 25 mA
- Low-power consumption



PIC 16F877

Peripheral Features:

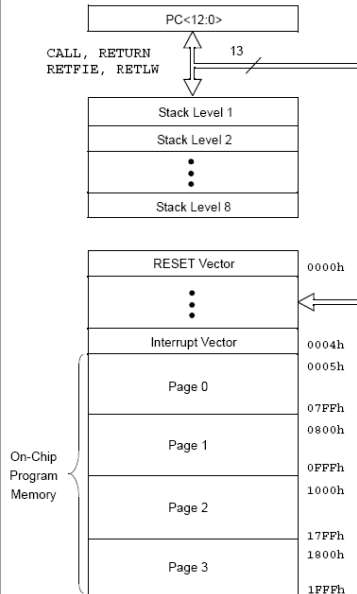
- Timer0: 8-bit timer/counter with 8-bit prescaler
- Timer1: 16-bit timer/counter with prescaler,
- Timer2: 8-bit timer/counter with 8-bit period register, prescaler and postscaler
- Two Capture, Compare, PWM modules
 - Capture is 16-bit, max. resolution is 12.5 ns
 - Compare is 16-bit, max. resolution is 200 ns
 - PWM max. resolution is 10-bit
- 10-bit multi-channel Analog-to-Digital converter
- Synchronous Serial Port (SSP) with SPI (Master mode) and I2C (Master/ Slave)
- Universal Synchronous Asynchronous Receiver Transmitter (USART/SCI)
- Parallel Slave Port (PSP) 8-bits wide
- Brown-out detection circuitry for Brown-out Reset (BOR)

PIC 16F877

Key Features PICmicro™ Mid-Range Reference Manual (DS33023)	PIC16F877
Operating Frequency	DC - 20 MHz
RESETS (and Delays)	POR, BOR (PWRT, OST)
FLASH Program Memory (14-bit words)	8K
Data Memory (bytes)	368
EEPROM Data Memory	256
Interrupts	14
I/O Ports	Ports A,B,C,D,E
Timers	3
Capture/Compare/PWM Modules	2
Serial Communications	MSSP, USART
Parallel Communications	PSP
10-bit Analog-to-Digital Module	8 input channels
Instruction Set	35 instructions

PIC 16F877

Program Memory Organization



- PIC16F877 has a 13-bit PC
- PIC16F877 has 8K x 14 words of FLASH program memory, and the
- Accessing a location above the physically implemented address will cause a wraparound.
- The RESET vector is at 0000h and the interrupt vector is at 0004h.

PIC 16F877

File Address	File Address	File Address	File Address
Indirect addr. ⁽¹⁾ 00h	Indirect addr. ⁽¹⁾ 80h	Indirect addr. ⁽¹⁾ 100h	Indirect addr. ⁽¹⁾ 180h
TMR0 01h	OPTION_REG 81h	TMR0 101h	OPTION_REG 181h
PCL 02h	PCL 82h	PCL 102h	PCL 182h
STATUS 03h	STATUS 83h	STATUS 103h	STATUS 183h
FSR 04h	FSR 84h	FSR 104h	FSR 184h
PORTA 05h	TRISA 85h		
PORTB 06h	TRISB 86h	PORTB 105h	TRISB 185h
PORTC 07h	TRISC 87h		
PORTD ⁽⁴⁾ 08h	TRISD ⁽⁴⁾ 88h		
PORTE ⁽⁵⁾ 09h	TRISE ⁽⁵⁾ 89h		
PCLATH 0Ah	PCLATH 8Ah	PCLATH 10Ah	PCLATH 18Ah
INTCON 0Bh	INTCON 8Bh	INTCON 10Bh	INTCON 18Bh
PIR1 0Ch	PIE1 8Ch	EEDATA 10Ch	EECON1 18Ch
PIR2 0Dh	PIE2 8Dh	EEADR 10Dh	EECON2 18Dh
TMR1L 0Eh	PCON 8Eh	EEDATH 10Eh	Reserved ⁽²⁾ 18Eh
TMR1H 0Fh		EEADRH 10Fh	Reserved ⁽²⁾ 18Fh
T1CON 10h			
TMR2 11h	SSPCON2 91h		
T2CON 12h	PR2 92h		
SSPBUF 13h	SSPADD 93h		
SSPCON 14h	SSPSTAT 94h		
CCPR1L 15h			
CCPR1H 16h			
CCP1CON 17h			
RCSTA 18h	TXSTA 98h		
TXREG 19h	SPBRG 99h		
RCREG 1Ah			
CCPR2L 1Bh			
CCPR2H 1Ch			
CCP2CON 1Dh			
ADRESH 1Eh	ADRESL 9Dh		
ADCON0 1Fh	ADCON1 9Fh		
20h	ADn A0h		
General Purpose Register 96 Bytes	General Purpose Register 80 Bytes	General Purpose Register 80 Bytes	General Purpose Register 80 Bytes
Bank 0 7Fh	accesses 70h-7Fh EFh FFh	accesses 70h-7Fh 16Fh 17Fh	accesses 70h-7Fh 1EFh 1FFh

Data Memory Organization

- The data memory is partitioned into multiple banks which contain the General Purpose Registers and the Special Function Registers.
- Bits RP1 (STATUS<6>) and RP0 (STATUS<5>) are the bank select bits.

RP1:RP0	Bank
00	0
01	1
10	2
11	3

PIC 16F877: A/D Converter Module

- 10-bit resolution
- 8 inputs
- Successive approximation A/D converter
- Selectable voltage reference sources (VDD, VSS, RA2, RA3)
- The A/D module has four registers.
 - A/D Control Register0 (ADCON0) → Control operation
 - A/D Control Register1 (ADCON1) → Config port pins
 - A/D Result High Register (ADRESH) → Store result
 - A/D Result Low Register (ADRESL) → Store result

PIC 16F877: A/D Module

ADCON0 REGISTER (ADDRESS: 1Fh)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0
ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/DONE	—	ADON
bit 7							bit 0

- ADCS1:ADCS0:** A/D Conversion Clock Select bits
 - 00 = FOSC/2
 - 01 = FOSC/8
 - 10 = FOSC/32
 - 11 = FRC (clock derived from the internal A/D module RC oscillator)
- CHS2:CHS0:** Analog Channel Select bits
 - 000 = channel 0, (RA0/AN0)
 - 001 = channel 1, (RA1/AN1)
 - 010 = channel 2, (RA2/AN2)
 - 011 = channel 3, (RA3/AN3)
 - 100 = channel 4, (RA5/AN4)
 - 101 = channel 5, (RE0/AN5)(1)
 - 110 = channel 6, (RE1/AN6)(1)
 - 111 = channel 7, (RE2/AN7)(1)

PIC 16F877: A/D Module

ADCON0 REGISTER (ADDRESS: 1Fh)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0
ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/DONE	—	ADON
bit 7							bit 0

- GO/DONE:** A/D Conversion Status bit
 - If ADON = 1:
 - 1 = A/D conversion in progress (setting this bit starts the A/D conversion)
 - 0 = A/D conversion not in progress (this bit is automatically cleared by hardware when the A/D conversion is complete)
- ADON:** A/D On bit
 - 1 = A/D converter module is operating
 - 0 = A/D converter module is shut-off and consumes no operating current

PIC 16F877: A/D Module

ADCON1 REGISTER (ADDRESS 9Fh)

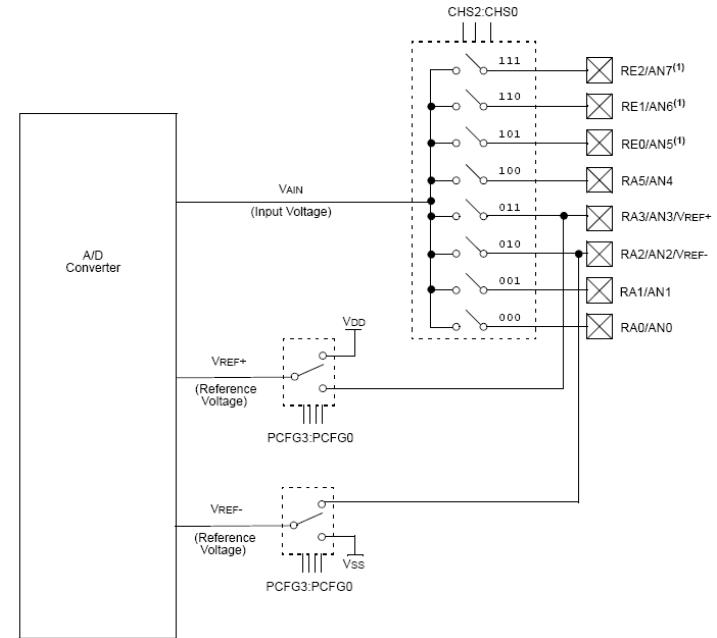
U-0	U-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
ADFM	—	—	—	PCFG3	PCFG2	PCFG1	PCFG0
bit 7				bit 0			

- **ADFM:** A/D Result Format Select bit
1 = Right justified. 6 Most Significant bits of ADRESH are read as '0'.
0 = Left justified. 6 Least Significant bits of ADRESL are read as '0'.
- **PCFG3:PCFG0:** A/D Port Configuration Control bits:

PCFG3: PCFG0	AN7 ⁽¹⁾ RE2	AN6 ⁽¹⁾ RE1	AN5 ⁽¹⁾ RE0	AN4 RA5	AN3 RA3	AN2 RA2	AN1 RA1	AN0 RA0	VREF+	VREF-	CHAN/ Refs ⁽²⁾
0000	A	A	A	A	A	A	A	A	VDD	VSS	8/0
0001	A	A	A	A	VREF+	A	A	A	RA3	VSS	7/1
0010	D	D	D	A	A	A	A	A	VDD	VSS	5/0
0011	D	D	D	A	VREF+	A	A	A	RA3	VSS	4/1
0100	D	D	D	D	A	D	A	A	VDD	VSS	3/0
0101	D	D	D	D	VREF+	D	A	A	RA3	VSS	2/1
011x	D	D	D	D	D	D	D	D	VDD	VSS	0/0
1000	A	A	A	A	VREF+	VREF-	A	A	RA3	RA2	6/2
1001	D	D	A	A	A	A	A	A	VDD	VSS	6/0
1010	D	D	A	A	VREF+	A	A	A	RA3	VSS	5/1
1011	D	D	A	A	VREF+	VREF-	A	A	RA3	RA2	4/2
1100	D	D	D	A	VREF+	VREF-	A	A	RA3	RA2	3/2
1101	D	D	D	D	VREF+	VREF-	A	A	RA3	RA2	2/2
1110	D	D	D	D	D	D	D	A	VDD	VSS	1/0
1111	D	D	D	D	VREF+	VREF-	D	A	RA3	RA2	1/2

A = Analog input D = Digital I/O

PIC 16F877 : A/D Module



PIC 16F877 : A/D Module

- The ADRESH:ADRESL registers contain the 10-bit result of the A/D conversion.
- When the A/D conversion is complete, the result is loaded into this A/D result register pair.
- The GO/DONE bit (ADCON0<2>) is cleared
- The A/D interrupt flag bit ADIF is set.
- The analog input channels must have their corresponding TRIS bits set as inputs.

PIC 16F877 : A/D Module

Using A/D Module

1. **Configure the A/D module:**
 - Configure analog pins/voltage reference and digital I/O (ADCON1)
 - Select A/D input channel (ADCON0)
 - Select A/D conversion clock (ADCON0)
 - Turn on A/D module (ADCON0)
2. **Configure A/D interrupt (if desired):**
 - Clear ADIF bit
 - Set ADIE bit
 - Set PEIE bit
 - Set GIE bit
3. **Wait the required acquisition time.**
4. **Start conversion:**
 - Set GO/DONE bit (ADCON0)
5. **Wait for A/D conversion to complete, by either:**
 - Polling for the GO/DONE bit to be cleared (with interrupts enabled); OR
 - Waiting for the A/D interrupt
6. **Read A/D result register pair (ADRESH:ADRESL), clear bit ADIF if required.**
7. **For the next conversion, go to step 1 or step 2, as required.**

PIC 16F877 : A/D Module

Obtaining A/D results

