Configuration Bits

CP	—	—	—	—	CPD	LVP	BOREN	MCLRE	FOSC2	PWRTE	WDTE	F0SC1	F0SC0
bit 13													bit 0

- The configuration bits can be programmed (read as ‘0’) or left unprogrammed (read as ‘1’) to set certain chip configurations.
- These bits are mapped in program memory location 2007h which is beyond the user program memory space.
- Special configuration memory space (2000h-3FFFh) can be accessed only during programming.

Configuration Bits

CP	—	—	—	—	CPD	LVP	BOREN	MCLRE	FOSC2	PWRTE	WDTE	F0SC1	F0SC0
bit 13													bit 0

bit 13: **CP:** Flash Program Memory Code Protection bit
1 = Code protection off
0 = 0000h to 07FFh code-protected

bit 8: **CPD:** Data Code Protection bit
1 = Data memory code protection off
0 = Data memory code-protected

bit 7: **LVP**: Low-Voltage Programming Enable bit
1 = RB4/PGM pin has PGM function, low-voltage programming enabled
0 = RB4/PGM is digital I/O, HV on MCLR must be used for programming

bit 6: **BOREN**: Brown-out Reset Enable bit
1 = BOR Reset enabled
0 = BOR Reset disabled

Configuration Bits

CP	—	—	—	—	CPD	LVP	BOREN	MCLRE	FOSC2	PWRTE	WDTE	F0SC1	F0SC0
bit 13													bit 0

bit 5: **MCLRE**: RA5/MCLR/VPP Pin Function Select bit
1 = RA5/MCLR/VPP pin function is MCLR
0 = RA5/MCLR/VPP pin function is digital Input, MCLR internally tied to VDD

bit 3: **PWRTE**: Power-up Timer Enable bit
1 = PWRT disabled
0 = PWRT enabled

bit 2: **WDTE**: Watchdog Timer Enable bit
1 = WDT enabled
0 = WDT disabled

Configuration Bits

CP	—	—	—	—	CPD	LVP	BOREN	MCLRE	FOSC2	PWRTE	WDTE	F0SC1	F0SC0
bit 13													bit 0

bit 4, 1-0: **FOSC<2:0>**: Oscillator Selection bits
111 = **RC oscillator**: CLKOUT function on RA6/OSC2/CLKOUT
110 = **RC oscillator**: I/O function on RA6/OSC2/CLKOUT
101 = **INTOSC oscillator**: CLKOUT function on RA6/OSC2/CLKOUT
100 = **INTOSC oscillator**: I/O function on RA6/OSC2/CLKOUT
011 = **EC**: I/O function on RA6/OSC2/CLKOUT, CLKIN on RA7/OSC1/CLKIN
010 = **HS oscillator**: High-speed crystal/resonator on RA6/OSC2/CLKOUT and RA7/OSC1/CLKIN
001 = **XT oscillator**: Crystal/resonator on RA6/OSC2/CLKOUT and RA7/OSC1/CLKIN
000 = **LP oscillator**: Low-power crystal on RA6/OSC2/CLKOUT and RA7/OSC1/CLKIN

Setting Configuration Bits

Configuration bits can be specified in source code by using a directive _ _ config as follows:

__**config** *configuration constants* ***&*** *……*

Configuration constants can be:

_CP_ON
_CP_OFF
_PWRTE_ON
_PWRTE_OFF
_WDT_ON
_WDT_OFF
_LP_OSC
_XT_OSC
_HS_OSC
_RC_OSC

Example

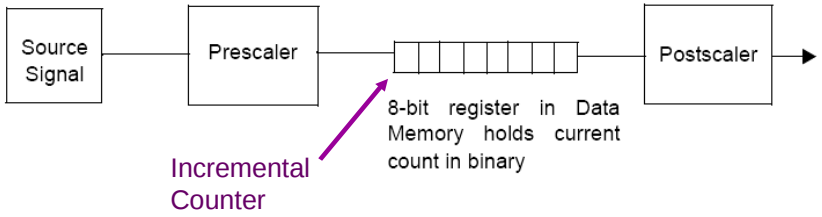
```
__config _CP_OFF & WDT_OFF &
_HS_OSC
```

Timer Module: TMR0

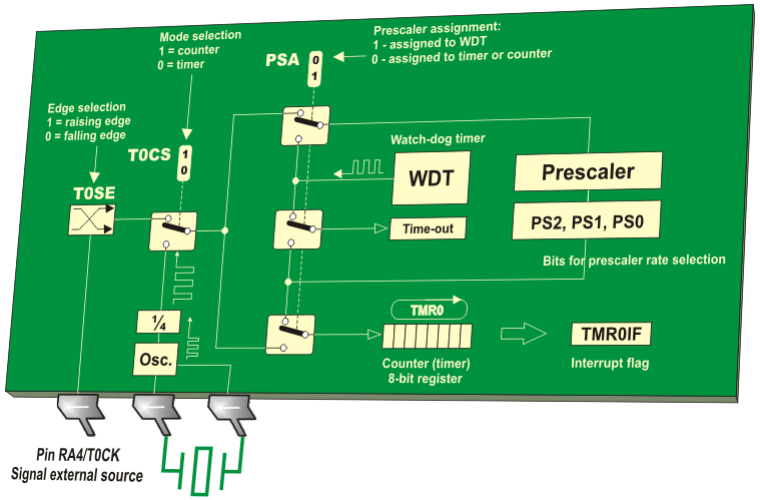
* Timer0 is an 8-bit Timer/Counter module with the following features:

  - 8-bit prescaler (shared with WDT).
  - Selectable internal or external clock source.
  - Interrupt on overflow (255→0).
  - Source edge selection (positive or negative going edge).

* To configure the Timer0 module the OPTION_REG Special Function Register (SFR) is used.



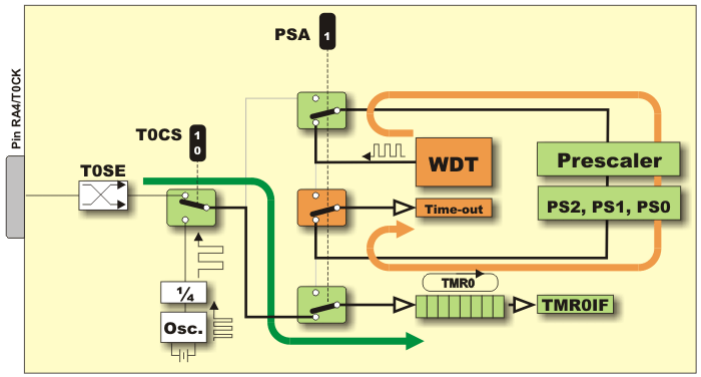
Timer Module: TMR0



Timer Module: TMR0

	R/W (1)	R/W (1)	R/W (1)	R/W (1)	R/W (1)	R/W (1)	R/W (1)	R/W (1)	Features
OPTION_REG	RBPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	Bit name
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	

T0CS: Timer0 Clock Source Select bit
1 = TMR0 receives clock signal from RA4/T0CKI pin
0 = TMR0 uses internal clock signal (Fosc/4)



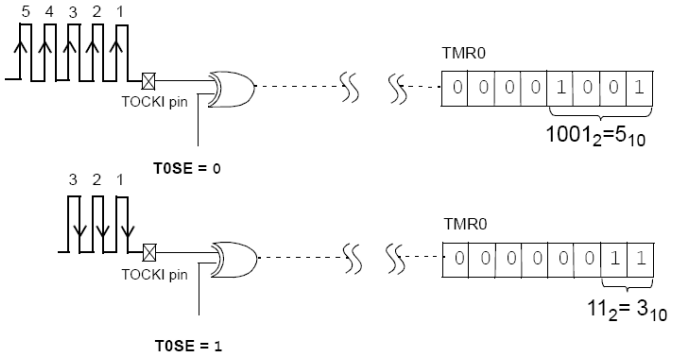
Timer Module: TMR0

OPTION_REG	R/W (1) RBPU Bit 7	R/W (1) INTEDG Bit 6	R/W (1) T0CS Bit 5	R/W (1) T0SE Bit 4	R/W (1) PSA Bit 3	R/W (1) PS2 Bit 2	R/W (1) PS1 Bit 1	R/W (1) PS0 Bit 0	Features / Bit name

T0SE: Timer0 Source Edge Select bit

1 = TMR0 register increments on high-to-low transition on T0CKI pin

0 = TMR0 register increments on low-to-high transition on T0CKI pin



Timer Module: TMR0

PRESCALER ASSIGNMENT AND CONFIGURATION

- The software programmable is available for use with either the Timer0 Watchdog Timer, but not both simultaneously.
- To assign the prescaler to Timer0, the Prescaler Assignment bit needs to be cleared.

OPTION_REG

				*PSA	PS2	PS1	PS0

*If PSA bit is SET (1), Prescaler is assigned to Watchdog Timer and PS2:PS0 have no effect (TMR0 RATE = 1:1)

PSA: Prescaler Assignment bit

1 = Prescaler is assigned to the Watchdog Timer module

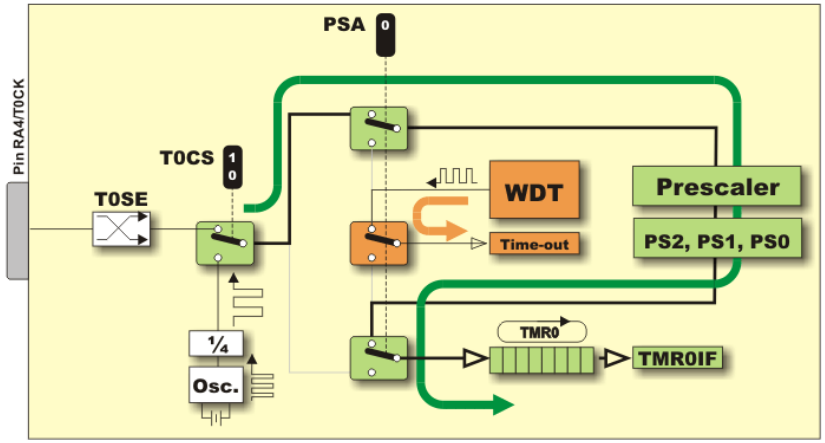
0 = Prescaler is assigned to Timer0 module

Timer Module: TMR0

The prescaler will determine how many source edges will increment the TMR0 register value by 1

PS2, PS1, PS0	*TMR0 RATE
000	1:2
001	1:4
010	1:8
011	1:16
100	1:32
101	1:64
110	1:128
111	1:256

Timer Module: TMR0



Timer Module: TMR0

- When the prescaler is assigned to the timer/counter, any write to the TMR0 register will clear the prescaler;
- When the microcontroller is setup in *sleep* mode, the oscillator is turned off. Overflow cannot occur since there are no pulses to count.
- When used as an external clock counter without prescaler, a minimal pulse length or a pause between two pulses must be 2 Tosc + 20 nS.
- When used as an external clock counter with prescaler, a minimal pulse length or a pause between two pulses is 10nS;

Timer Module: TMR0

To select mode:

- Timer mode is selected by the T0CS bit of the OPTION_REG register
- The prescaler should be assigned to the timer by clearing the PSA bit of the OPTION_REG register.
- The prescaler rate is set by using the PS2-PS0 bits of the same register
- When using interrupt, the GIE and TMR0IE bits of the INTCON register should be set.

Timer Module: TMR0

To measure time:

- Reset the TMR0 register or write a known value to it;
- Elapsed time (in uS) is measured by reading the TMR0 register (Fosc = 4 MHz)
- The flag bit TMR0IF of the INTCON register is automatically set every time the TMR0 register overflows. If enabled, an interrupt occurs.

Timer Module: TMR0

To count pulses:

- The polarity of pulses are to be counted is selected on the RA4 pin are selected by the TOSE bit of the OPTION register
- Number of pulses can be read from the TMR0 register.
  The prescaler and interrupt are used in the same manner as in timer mode.

Timer Module: TMR0

Design Example