#### **IEEE 1284**

#### Bi-directional parallel communications standard

IEEE 1284 can operate in five modes:

- <u>Compatibility Mode</u>, also known as *Centronics*, standard or SPP, is a uni-directional implementation.
- <u>Nibble Mode</u> is a uni-directional interface that allows the device to transmit data four bits at a time using status lines for data.
- Byte Mode allows the device to transmit 8 bits at a time using data lines.
- Enhanced Parallel Port (EPP) is a half-duplex bi-directional interface designed to allow devices to transmit large amounts of data.
- Extended Capability Port (ECP) is a half-duplex bi-directional interface similar to EPP, except that PC implementations use DMA to provide faster data transfer than EPP.

### **Port Addresses**

Traditionally IBM PC systems have allocated their first three parallel ports according to the configuration in the table below.

PORT NAME	Interrupt #	Starting I/O	Ending I/O
LPT1	IRQ 7	378h	37fh
LPT2	IRQ 7	278h	27fh
LPT3	IRQ 5	3bch	3bfh

## **Connector Types**







### **Pinouts**

Bit to Pin Mapping for the Standard Parallel Port (SPP):

Address		MSB							LSB
	Bit:	7	6	5	4	3	2	1	0
Base (Data port)	Pin:	9	8	7	6	5	4	3	2
Base+1 (Status port)	Pin:	~11	10	12	13	15			
Base+2 (Control port)	Pin:					~17	16	~14	~1

~ indicates a hardware inversion of the bit.

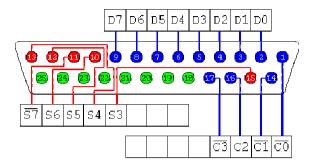
### **Pinouts**

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Pin No (DB25)	Signal name	Direction	Register - bit	Inverted				
1	nStrobe	Out	Control-0	Yes				
2	Data0	In/Out	Data-0	No				
3	Data1	In/Out	Data-1	No				
4	Data2	In/Out	Data-2	No				
5	Data3	In/Out	Data-3	No				
6	Data4	In/Out	Data-4	No				
7	Data5	In/Out	Data-5	No				
8	Data6	In/Out	Data-6	No				
9	Data7	In/Out	Data-7	No				
10	nAck	In	Status-6	No				
11	Busy	In	Status-7	Yes				
12	Paper-Out	In	Status-5	No				
13	Select	In	Status-4	No				
14	Linefeed	Out	Control-1	Yes				
15	nError	In	Status-3	No				
16	nInitialize	Out	Control-2	No				
17	nSelect-Printer	Out	Control-3	Yes				
18-25	Ground	-	-	-				

#### **Pinouts**

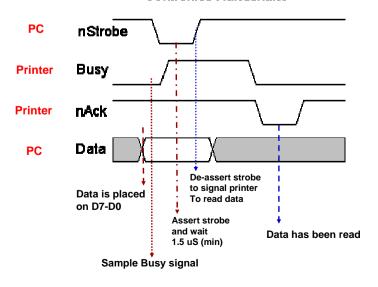
The original IBM-PC's Parallel Printer Port had a total of 12 digital outputs and 5 digital inputs accessed via 3 consecutive 8-bit ports in the processor's I/O space.

- 8 output pins accessed via the **DATA Port**
- 5 input pins (one inverted) accessed via the **STATUS Port**
- 4 output pins (three inverted) accessed via the CONTROL Port
- The remaining 8 pins are grounded

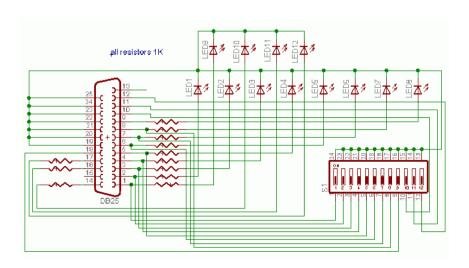


# Signals diagram

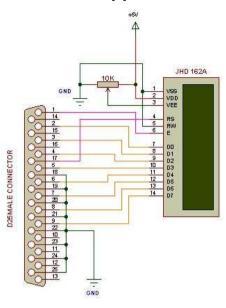
#### **Centronics Handshake**



# **Applications: Simple I/O (SW & LED)**



# **Applications: Parallel port LCD**







# **Applications: 8255 Interfacing**

