8255 Programmable Peripheral Interface

- The Intel 8255A is a general purpose programmable I/O device which is designed for use with all Intel and most other microprocessors.
- It provides 24 I/O pins which may be individually programmed in 2 groups of 12 and used in 3 major modes of operation.
- ullet The 8255 is a 40 pin integrated circuit (IC), designed The 8255 is a 40 pin IC designed by Intel for the 8080 microprocessor.

Pin Configuration

PA3

D0 - D7 These are the data input/output lines for the device. All information read from and written to the 8255 occurs via these 8 data lines.

CS (Chip Select Input). If this line is a logical 0, the microprocessor can read and write to the 8255.

RD (Read Input) Whenever this input line is a logical 0 and the RD input is a logical 0, the 8255 data outputs are enabled onto the system data bus.

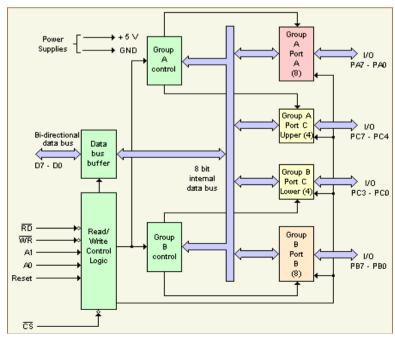
WR (Write Input) Whenever this input line is a logical 0 and the CS input is a logical 0, data is written to the 8255 from the system data bus

A0 - A1 (Address Inputs) The logical combination of these two input lines determines which internal register of the 8255 data is written to or read from.

RESET The 8255 is placed into its reset state if this input line is a logical 1. All peripheral ports are set to the input mode.

PAO - PA7, PBO - PB7, PCO - PC7 These signal lines are used as 8-bit I/O ports.

Block Diagram

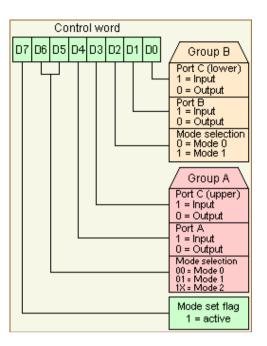


Port Selection

ADDRESS: These input signals, in conjunction $\overline{\text{RD}}$ and $\overline{\text{WR}}$, control the selection of one of the three ports or the control word registers.

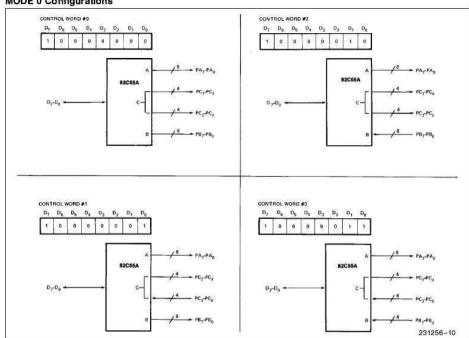
A ₁	A ₀	RD	WR	CS	Input Operation (Read)
0	0	0	9	0	Port A - Data Bus
10000	4	7520	140	7 3	2004 CAR (60) - WHOM CAR (60)
0		0	1	0	Port B - Data Bus
=1	0	0	1	0	Port C - Data Bus
4	1	0	11	0	Control Word - Data Bus
	N		x	000	Output Operation (Write)
0	0	7	0	0	Data Bus - Port A
0	1	1	0	0	Data Bus - Port B
1	0	14	0	0	Data Bus - Port C
1	1	1	0	0	Data Bus - Control

Control Word Register

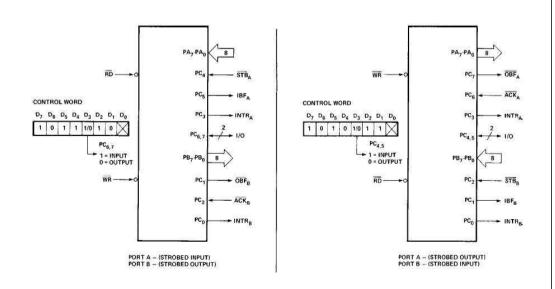


Mode 0 : Basic Input/Output

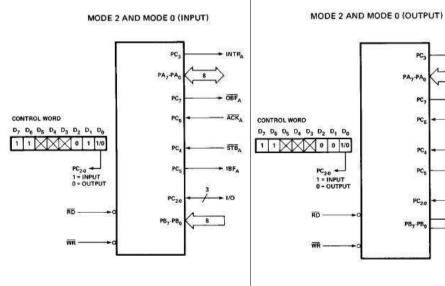
MODE 0 Configurations



Mode 1 : Strobed Input/Output



Strobed Bidirectional Bus I/O



- INTRA

Mode Definition Summary

	MODE 0		
	IN	OUT	
PA ₀	IN	OUT	
PA ₁	IN	OUT	
PA ₂	IN	OUT	
PA ₃	IN	OUT	
PA ₄	IN	OUT	
PA ₅	IN	OUT	
PA ₆	IN	OUT	
PA ₇	IN	OUT	
PB ₀	IN	OUT	
PB ₁	IN	OUT	
PB ₂	IN	OUT	
PB ₃	IN	OUT	
PB ₄	IN	OUT	
PB ₅	IN	OUT	
PB ₆	IN	OUT	
PB ₇	IN	OUT	
PC ₀	IN	OUT	
PC ₁	IN	OUT	
PC ₂	IN	OUT	
PC ₃	IN	OUT	
PC ₄	IN	OUT	
PC ₅	IN	OUT	
PC ₆	IN	OUT	
PC ₇	IN	OUT	

MODE 1				
IN	OUT			
INTRB	INTRB			
IBF _B	OBF _B ACK _B			
STBB	INTRA			
STB _A	I/O			
	1/0			
IBF _A	ACKA			
1/0	OBFA			

MODE 2				
GROUP A ONLY				
\longleftrightarrow				
3 3				
(200				
				
				
S				
() ()				
(2000)				
I/O I/O I/O INTR _A STB _A IBF _A ACK _A OBF _A				