Chapter 6
Solving Larger
Sequential Systems

- Shift Registers
- Counters
- Programmable Logic Devices (PLD)
- Hardware Design Languages

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Shift Register

- data is often stored in *registers*, rather than individual flip-flops.

- A register is just a collection of flip-flops, often with a common name (using subscripts to indicate the individual flip-flops) and usually with a common clock.

- A *shift register* is a set of flip-flops, such that the data moves one place to the right on each clock or shift input.

A simple shift register and its timing trace
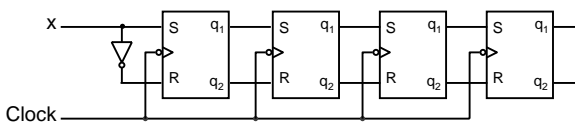
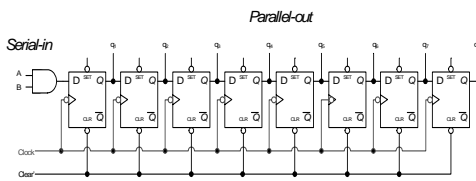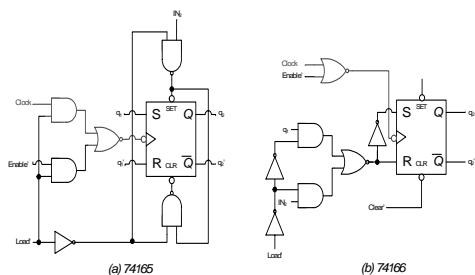| x	1	0	1	1	1	0	1	1	1	1	0	0	0				
Q_1	0	1	0	1	1	1	0	1	1	1	1	0	0	0			
Q_2	0	0	1	0	1	1	1	0	1	1	1	1	0	0	0		
Q_3	0	0	0	1	0	1	1	1	0	1	1	1	1	0	0	0	
Q_4	0	0	0	0	1	0	1	1	1	0	1	1	1	1	0	0	0

Shift Register (cont.)

- Serial-in / Parallel-in Shift Registers

- Serial-out / Parallel-out Shift Registers

- Right / Left Shift Registers

- Leading-edge / Trailing-edge Shift Registers

- *Enable, Clear, Load pins*

74164
Serial-in parallel-out shift register

Parallel-in Shift Register

(a) 74165

loading is done statically

(b) 74166

loading is done synchronously

Table 6.1 Right/left shift register.

	Clear'	S_0	S_1	q_1^+	q_2^+	q_3^+	q_4^+
Static clear	0	X	X	0	0	0	0
Hold	1	0	0	q_1	q_2	q_3	q_4
Shift left	1	0	1	q_2	q_3	q_4	LS
Shift right	1	1	0	RS	q_1	q_2	q_3
Load	1	1	1	IN_1	IN_2	IN_3	IN_4

Figure 6.7 Right/left shift register.

Figure 6.8 The 74161 counter.

Figure 6.9 8-bit counter.

8-bit counter from two 74161 counters
can count to 255 (2^8 - 1)
12-bit counter from three 74161 counters
can count to 4095 (2^{12} - 1)

Figure 6.10 Typical bit of the 74191 Down/Up' counter.

Figure 6.11 The 74191 Down/Up' counter.

LD'	EN'	D/U'	
0	X	X	Static load
1	1	X	Do nothing
1	0	0	Clocked count up
1	0	1	Clocked count down

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Programmable Logic Devices (PLD)

- Since sequential system is a combination of memory and combinational logic, it can be implemented using any of the programmable logic devices of Chapter 4 (for the combinational logic) and some flip-flops (for the memory).
- There are a variety of devices commercially available that combine primarily a PAL and some D flip-flops. There are also some very complex programmable devices available.

Figure 6.13 One output of a 16R8 PLD.

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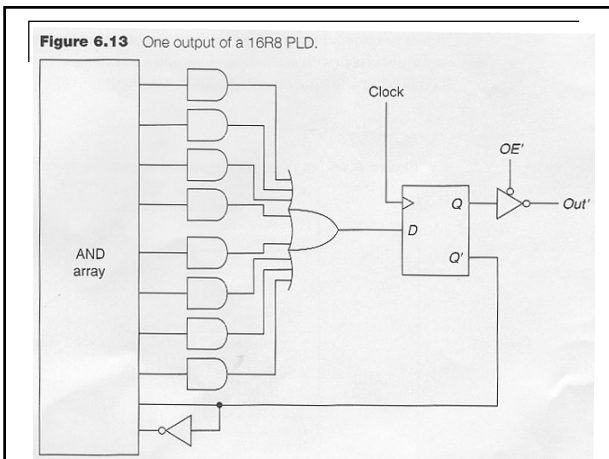
Design using ASM diagrams

- ASM (algorithmic state machine) is the same as sequential system.

- A tool is cross between a state diagram and a flow chart is the ASM diagram.

Figure 6.16a State box. Figure 6.16b Decision box. Figure 6.16c Mealy output box.

Figure 6.17 An ASM block.

Figure 6.18 Moore state diagram and ASM diagram.

Figure 6.19 Mealy state diagram and ASM diagram.

Hardware Design Languages (HDLs)

Figure 6.20 A full adder.

Verilog structural description of a full adder

```
module full_adder (c_out, s, a, b, c);
   input a, b, c;
   wire a, b, c;
   output c_out, s;
   wire c_out, s;
   wire w1, w2, w3;
   xor x1 (w1, a, b);
   xor x2 (s, w1, c);
   nand n1 (w2, a, b);
   nand n2 (w3, w1, c);
   nand n3 (c_out, w3, w2);
endmodule
```

Behavioural Verilog
for the full adder

```
module full_adder (c_out, s, a, b c);
   input a, b, c;
   wire a, b, c;
   output c_out, s;
   reg c_out, s;
   always
      begin
         s = a^b^c;
         c_out = (a&b) | (a&c_in) | (b&c_in);
      end
endmodule
```

(a) With logic equations

(b) With algebraic equations

```
module full_adder (c_out, s, a, b c);
   input a, b, c;
   wire a, b, c;
   output c_out, s;
   reg c_out, s;
   always
      begin
         s = a^b^c;
         {c_out, s} = a + b + c;
      end
endmodule
```